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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,633	10/10/2003	Nadeem N. Eleyan	004-7986	1194

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EXAMINER	
AUDUONG, GENE NGHIA	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/683,633	NADEEM N. ELEYAN, ET AL.	
	Examiner	**Art Unit**	
	Gene N. Auduong	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-68 is/are pending in the application.
  4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) 1-68 is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  a)☐ All b)☐ Some * c)☐ None of:
    1.☐ Certified copies of the priority documents have been received.
    2.☐ Certified copies of the priority documents have been received in Application No. _____.
    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3-8-04 & 1-11-05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on March 8, 2004 and January 11, 2005 is being considered by the examiner.

Claim Objections

2. Claims 2-7 are objected to because of the following informalities:

- Claim 2, line 2, the limitation "the selective exposure" is insufficient antecedent basis for this limitation in the claim. Is it the same with the limitation "selectively exposing one of the transistor to a bias voltage"?
- Claims 3-7 are depending on claims 2, which are being objected to.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

4. Claims 1-68 are rejected under 35 U.S.C. 102(b) as being anticipated by Proebsting U.S. Pat. No. 6,462,998.

Regarding claim 1, Proebsting discloses a memory circuit comprising: a sense circuit including a cross-coupled pair of transistors (col. 7, lines 29+); and a control block (figure 1n control block 112) responsive to detection of sensing offset of the sensing circuit, the control block at least partially compensating for the detected sensing offset by selectively exposing one of the transistors to a bias voltage selected to cause a compensating shift in a characteristic of the exposed transistor (col. 3, lines 4+).

Regarding claim 2, as best understood, Proebsting discloses the memory circuit as of claim 1, wherein the selective exposing transistor include purposeful instruction, into the sensing circuit, of a data pattern having a predominate value selected to introduce data dependent creep in the characteristic of the exposed transistor (col. 8, lines 41+; col. 28, lines 27+).

Regarding claims 3-7, Proebsting discloses the memory circuit as of claim 2, wherein the data pattern is introduced directly to sensing circuit; is interspersed amongst memory cell data sensed by the sensing circuit; consists of sequence of predominate value; and wherein the offset data dependent creep is associated with negative bias temperature instability (col. 9, lines 38+).

Regarding claim 8, Proebsting discloses the memory circuit as of claim 1, wherein the transistors are PMOS device (col. 7, lines 29+).

Regarding claim 9, Proebsting discloses the memory circuit as of claim 1, wherein the shifted characteristic of the exposed transistor includes its threshold voltage (col. 10, lines 6; col. 28, lines 27+).

Regarding claim 10, Proebsting discloses the memory circuit as of claim 1, wherein the sensing offset results, at least in part, from an effect that disparately affects one of the pair of transistors as compared with the other, the disparate effect based on a skew in a history of values read out from associated memory elements (col. 8, lines 41+).

Regarding claims 11 and 14, Proebsting discloses the memory circuit as of claim 10, wherein the disparate effect is associated with negative bias temperature instability (col. 27, lines 38+; col. 28, lies 27+).

Regarding claims 12-13, Proebsting discloses the memory circuit as of claim 1, wherein the sensing offset results, at least in part, from an accumulated data dependent mismatch in characteristic of the cross-coupled transistors are coupled (col. 13, lines 19+).

Regarding claims 15-17, Proebsting discloses the memory circuit as of claim 1, further comprising a test block configured to detect the sensing offset; selectively introduced discharge paths into respective balanced/imbalanced discharge paths allowing the test block to characterize a direction of the sense offset (col. 13, lines 30+).

Regarding claim 18, Proebsting discloses the memory circuit as of claim 1, further comprising: a test block that selectively introduces a calibrated imbalance into a differential circuit sensing circuit, the calibrated imbalance allowing the test block to characterize the sensing offset (col. 35, lines 38+; col. 39, lines 4+).

Regarding claims 19-21, Proebsting discloses the memory circuit as of claim 1, wherein the control block is responsive to an in situ test operation that characterizes the sensing offset (col. 13, lines 26+; col. 46, lines 56+).

Regarding claims 22-25, Proebsting discloses the memory circuit as of claim 1, embodiment in computer readable descriptive form suitable for use in design test or fabrication of an integrated circuit (col. 8, lines 41+; col. 10, lines 25+).

Claims 51-60 and 61-68 contain the similar limitation as previously discussed in claims 1-25. Therefore, they are analyzed as previously discussed with respect to claims 1-25.

Regarding claims 26-43 and 44-50, the apparatus as previously discussed in claims 1-25, 51-68 would be performed the method as claimed. Therefore, they are analyzed as previously discussed with respect to apparatus claims 1-25 and 51-68.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
May 17, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827